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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,225	06/09/2000	David Robert Baldwin	TD-155	3467

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BOX 802889
DALLAS, TX 75380-2889

EXAMINER	
TUNG, KEE M	
ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 06/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,225	BALDWIN, DAVID ROBERT	
	Examiner	Art Unit	
	Kee M. Tung	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,15,17 and 20* is/are allowed.

6)☒ Claim(s) *1-5,7-13,16 and 19* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the Appeal Brief filed on 4/25/05, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. For future Appeal, there are a few things need to be correct in the brief:

The brief needs to include a statement of **Grouping of the Claims** as required under 37 CFR 1.192(c)(7). MPEP § 1206.

Also is required to submit a separate amendment to cancel a claim (Claim 11 never been cancelled).

And, should included all arguments related to claim rejected under 35 USC 112 (claim 2).

Claim Rejections - 35 USC § 112

3. Claims 2 and 8-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As per claim 2, line 3, the phrase "... **from dedicated graphics memory into a main memory**" is not described nor shown in the drawing. The specification only teaches "graphics accelerator unit manages page faulting of texture data **from main memory into a dedicated graphics memory**".

As per claim 11, the claimed "CPU **includes** a user input device, a microprocessor, and a data output device" is not described nor shown in the drawings.

4. Claim 7 recites the limitation "said graphics memory manager" in lines 8-9 and 11. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuyabu et al (6,297,832 hereinafter "Mizuyabu") in view of Slaughter et al (6,202,146 hereinafter "Slaughter").

As per claim 1, Mizuyabu teaches a computer system (Fig.1 shows a video graphics system that is utilized in an application such as a set-top box (col. 4, lines 1-3)

which is or can be a part of the computer system) comprising a graphics accelerator unit (Fig. 1, video graphics system) which manages page faulting (memory controller 20 manages page faults, col. 5, lines 1-3) of texture data (shows texture data also stored in the memory 10, col. 4, lines 55-58) invisibly to the host processor (Fig. 1 shows the memory controller 20 coupled between memory 10 and a plurality of memory clients and does not involved host processor and thus is considered invisible to the host processor). Since applicant argues Mizuyabu cannot be a computer system, the examiner introduces a new prior art to Slaughter to show that a set-top box is considered as a computer system or part of a computer system (see col. 4, lines 21-33 and Fig. 1). The computer system of Slaughter comprises a CPU (102), a main memory (104), a system bus (106), a DMA controller (116) and I/O devices (108-112). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Slaughter into the system of Mizuyabu in order to support that a set-top box of Mizuyabu is considered as a computer system and the computer system includes a CPU. Therefore, at least claim 1 would have bee obvious.

As per claim 3, the combined system teaches a computer system (Mizuyabu, Fig.1 shows a video graphics system which is a part of the computer system and Slaughter, Fig. 1) comprising at least one CPU (Mizuyabu ,not shown in Fig. 1, but is inherent to any well known computer system to include at least one CPU and Slaughter,102), operatively connected to have read/write access to a main memory (Mizuyabu, also not shown in Fig. 1 but is also inherent to any well known computer

system to include a main memory, Slaughter, 104); first memory management logic (also not shown in Fig. 1, but is also inherent to any well known computer system to include MMU to manage virtual memory), which virtualizes said main memory with reference to at least one bulk storage unit (Slaughter, such, as, disk memory 114, by definition from Microsoft Press Computer Dictionary, virtual memory may be partially simulated by secondary storage such as a hard disk); a graphics accelerator unit (Fig. 1, video graphics system), comprising rendering accelerator logic (Mizuyabu, Fig. 1, 3D/2D graphics image processor 70 and 80), dedicated graphics memory (Mizuyabu, memory 10), and a second memory management unit (Mizuyabu, memory controller 20) which manages texture data (Mizuyabu shows texture data also stored in the memory 10, col. 4, lines 55-58) for said accelerator logic and performs page faulting (Mizuyabu, memory controller 20 manages page faults, col. 5, lines 1-3) of said texture data, invisibly to the host processor (Mizuyabu, Fig. 1 shows the memory controller 20 coupled between memory 10 and a plurality of memory clients and does not involved host processor and thus is considered invisible to the host processor). Therefore, at least claims 3 and 13 would have been obvious by Mizuyabu and Slaughter.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuyabu et al (6,297,832 hereinafter "Mizuyabu") and Slaughter et al (6,202,146 hereinafter "Slaughter") in view of Porterfield (6,249,853).

The teachings of Mizuyabu and Slaughter are given in previous paragraph of this Office action. However, Mizuyabu and Slaughter fail to explicitly suggest or teach said first memory management logic is a bridge controller. This is what Porterfield teaches

(Fig. 3, system logic 154 includes a main memory controller to control/manage the access of the main memory 156, col. 6, lines 22-24). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Porterfield into the combined system of Mizuyabu and Slaughter in order to manage or control the access of the main memory in efficient and effective manner. Therefore, at least claim 12 would have been obvious.

8. Claims 4, 5, 7, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peddada et al (6,295,068 hereinafter "Peddada") in view of Duluk, Jr. et al (6,288,730 hereinafter "Duluk").

As per claim 4, Peddada teaches a computer system (Fig. 5) comprising a host processor (CPU 10) having host physical memory (main memory 12) associated therewith, and a graphics accelerator unit (3D graphics accelerator 20) having respective local memory (memory 22 and 24) associated therewith; wherein, when said graphics accelerator unit attempts to access texture data which is in said physical memory associated with said host, said graphics memory manager fetches said texture data automatically (col. 6, lines 22-39, by using DMA transfer engine in the graphics accelerator 20). However, Peddada fails to explicitly teach the graphics accelerator unit also having a graphics memory manager. Peddada teaches a 3D graphics driver (60) to manage the texture data. Duluk teaches a deferred graphics pipeline processor (abstract, Fig. 2 shows part of the processor, a texture unit 1200 and col. 8, line 19 through col. 9, line 13) includes a texture setup (1211), a texture memory (1213), a prefetch buffer control (1218), a texture MMU (1210), a frame buffer (21), AGP memory

(1222), a virtual memory (1223), a disk memory (1224), memory queue (1219), a texel prefetch buffer (1216) and a texture interpolator (1218). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Duluk into the system of Peddada in order to more efficiently accessing the texture data and thus increase the performance of the graphics system.

As per claim 5, Peddada teaches after fetching said texture data, said graphics memory manager restarts texture processing (col. 5, lines 30-40).

As per claim 7, Peddada teaches a computer system (Fig. 5) comprising a host processor (CPU 10) having host physical memory (main memory 12) associated therewith, and also having virtual memory management (not shown in the figures, but is inherent to any well known computer system to include a MMU in the processor to manage virtual memory, further see Duluk for virtual memory 1223 and disk memory 1224); and a graphics accelerator unit (3D graphics accelerator 20) having respective physical memory (memory 22 and 24) associated therewith, and also having a virtual memory management (see rejection on claim 4 above, such as, texture MMU 1210 and virtual memory 1223 to disk memory 1224 in Duluk); and wherein, when said graphics accelerator unit attempts to access texture data which is in said host physical memory, if said texture data is in said host physical memory, said graphics memory manager fetches said texture data therefrom automatically (col. 6, lines 22-39); and if said texture data is not in said host physical memory, said texture data is first loaded into said host physical memory, and thereafter said graphics memory manager fetches said texture

data automatically from said host physical memory (col. 5, lines 61-67 and col. 6, lines 14-39). Therefore, at least claim 7 would have been obvious.

As per claims 16 and 19, Peddada teaches said host processor is operatively connected to receive inputs from input devices (inherently, such as, mouse, keyboard) through an interface manager chip (system logic chipset 16) which provides an interface to various ports and register.

9. Claims 2 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuyabu et al (6,297,832 hereinafter "Mizuyabu") and Slaughter et al (6,202,146 hereinafter "Slaughter") in view of Peddada et al (6,295,068 hereinafter "Peddada").

Note. The claim is interpolated as "manages page faulting of texture date from main memory into dedicated graphics memory".

The teachings of Mizuyabu and Slaughter are given in previous paragraph of this Office action. However, Mizuyabu and Slaughter fail to explicitly suggest or teach "manages page faulting of texture date from main memory into dedicated graphics memory". This is what Peddada teaches (Fig. 5, col. 6, lines 22-39, by using DMA transfer engine in the graphics accelerator 20 to copy texture data from AGP memory 14 into texture cache 24). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Paddada into the combined system of Mizuyabu and Slaughter in order to manage or control the access of the main memory in efficient and effective manner by using DMA transfer engine. Therefore, at least claim 2 would have been obvious.

As per claim 8, Paddada teaches said graphics accelerator unit also includes a PCI/AGP interface (interface to AGP 26), DMA controller (DMA transfer engine, col. 6, line 34), SGRAM/SDRAM (obvious in view of frame buffer 22), a RAMDAC (inherent in view of 3D engine 20 and Display 30 in Fig. 5), and a video stream interface (Mizuyabu, Fig. 1 shows video engine 40 and processor 60).

As per claim 9, Paddada teaches said dedicated graphics memory is SGRAM/SDRAM to which the unit has read/write access through its frame buffer and local buffer ports (obvious in view of dual port frame buffer 22 to replace by SGRAM/SDRAM type memory).

As per claim 10, Slaughter teaches said host processor (102) is operatively connected to receive inputs from input devices (108 and 110) through an interface manager chip (not shown, but would have been obvious in view of the bus 106 in order to manage the access of bus 106 or bus manager 228 in Fig. 2) which provides an interface various ports and registers.

Response to Arguments

10. Applicant's arguments filed 4/25/05 have been fully considered but they are not persuasive.

The rejections have been modified in order to fully considered applicant's arguments.

Regarding prior art to Mizuyabu, applicant argues that Mizuyabu does not teach a host processor. A new prior art was introducing into the rejection. Applicant further argues that the definition of page fault is different. However, the claim merely requires a

page fault without further definition. The specification is not the measure of invention. Therefore, limitations contained therein can be read into the claims for the purpose of avoiding prior art. In re Sporck, 55 CCPA 743, 386 F 2d 924, 155 USPQ 687 (1968).

Regarding prior art to Paddada, applicant's argument is moot in view of new rejection.

Regarding prior art to Emberling, the prior art has been withdrawn.

Allowable Subject Matter

11. Claims 14, 15, 17 and 20 are allowed.

12. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gauthier (5,594,860) teaches a printer controller system comprising a graphics processing unit (GPU 18) includes virtual memory management capabilities.

Brotz (6,374,404) teaches a set-top box (112) at least includes a CPU (101), main memory (102 and 103) and rendering engine (118).

Polit et al (6,407,998) teaches a set-top box system which combine PC and TV functions are increasingly becoming generic (col. 1, lines 15-20).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M. Tung whose telephone number is 571-272-7794. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2671